Form PTO-1449 (Modified)

**INFORMATION DISCLOSURE STATEMENT BY APPLICANT**
(Use several sheets if necessary)

| Atty. Docket No. | Serial No. |
|---|---|
| 1662-37500 (P00-3162) | Not Yet Assigned |
| **Applicant** | |
| Shubhendu S. MUKHERJEE | |
| **Filing Date** | **Group** |
| Concurrently Herewith | Unknown |

**REFERENCE DESIGNATION U.S. PATENT DOCUMENTS**

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB-CLASS | FILING DATE IF APPROPRIATE |
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**FOREIGN PATENT DOCUMENTS**

| | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB-CLASS | Translation YES | Translation NO |
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**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

| | | |
|---|---|---|
| SG | AA | *AR-SMT: Microarchitectural Approach To Fault Tolerance In Microprocessors*, Eric Rotenberg, (8 p.). |
| SG | AB | *DIVA: A Dynamic Approach To Microprocessor Verification*, Todd M. Austin, Journal of Instruction-Level Parallelism 2 (2000) 1-6, Submitted 2/2000; published 5/2000 (26 p.). |
| SG | AC | *DIVA: A Reliable Substrate For Deep Submicron Microarchitecture Design*, Todd M. Austin, May/June 1999 (12 p.). |
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**EXAMINER** Shane Smith **DATE CONSIDERED** 3/2/04

**EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.**

Form PTO-1449 (Modified)

**INFORMATION DISCLOSURE STATEMENT BY APPLICANT**
(Use several sheets if necessary)



| Atty. Docket No. | Serial No. |
|---|---|
| 1662-37500 (P00-3162) | 09/839,624 |
| **Applicant** | |
| Shubhendu S. MUKHERJEE | |
| **Filing Date** | **Group** |
| April 19, 2001 | 2183 |



**REFERENCE DESIGNATION U.S. PATENT DOCUMENTS**

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB-CLASS | FILING DATE IF APPROPRIATE |
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| 3/2/04 SG | AA | 5,758,142 | 05/26/98 | McFarling et al. | 395 | 586 | 05/31/94 |
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**FOREIGN PATENT DOCUMENTS**

| | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB-CLASS | Translation YES | NO |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |



**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

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|---|---|---|
| SG | AC | M. Franklin, "Incorporating Fault Tolerance in Superscalar Processors," Proceedings of High Performance Computing, December, 1996. |
| SG | AD | A. Mahmood et al., "Concurrent Error Detection Using Watchdog Processors - A Survey," IEEE Trans. on Computers, 37(2):160-174, February 1988. |
| SG | AE | J. H. Patel et al., "Concurrent Error Detection In ALU's by Recomputing With Shifted Operands," IEEE Trans. on Computers, 31(7):589-595, July 1982. |
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| SG | AJ | J. E. Smith et al., "Implementing Precise Interrupts In Pipelined Processors," IEEE Trans. on Computers, 37(5):562-573, May 1988. |
| SG | AK | G. S. Sohi et al., "A Study Of Time-Redundant Fault Tolerance Techniques For High-Performance Pipelined Computers," Digest of Papers, 19th International Symposium on Fault-Tolerant Computing, pp. 436-443, 1989. |
| SG | AL | G. S. Sohi et al., "Instruction Issue Logic For High-Performance, Interruptible, Multiple Functional Unit, Pipelined Computers," IEEE Transactions on Computers, 39(3):349-359, March 1990. |
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| SG | AP | L. Spainhower et al., "IBM S/390 Parallel Enterprise Server G5 Fault Tolerance: A Historical Perspective," IBM J. Res. Develop. Vol. 43, No. 5/6, September/November 1999, pp. 863-873. |
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| SG | AR | K. Sundaramoorthy et al., "Slipstream Processors: Improving Both Performance And Fault Tolerance" (6 p.). |

| EXAMINER | DATE CONSIDERED |
|---|---|
| Shawn Doost | 3/2/04 |

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